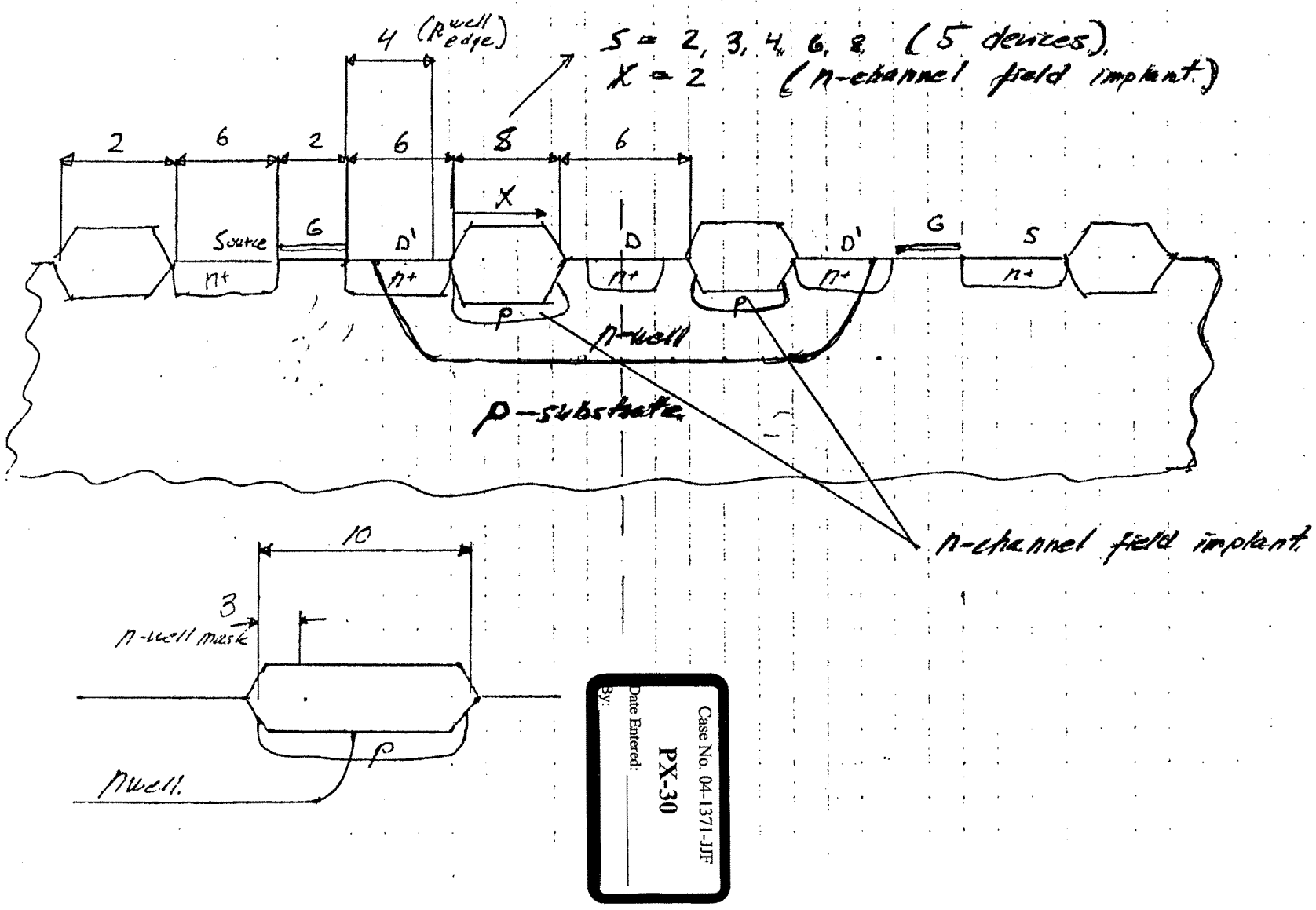
Exhibit A

Wm. H. Eklund 1, -85.

High voltage MOS device

n-channel cascoded with pinch resistor

W = 100 μm.



Case No. 04-1371-JJF
PX-30
Date Entered: _____
By: _____

Wm. H. Eklund -85

High voltage MOS device

N-channel with n-well drain cascoded with pinch resistor

S = 2, 3, 4, 6, 8.
X = 2 (n-channel field implant)

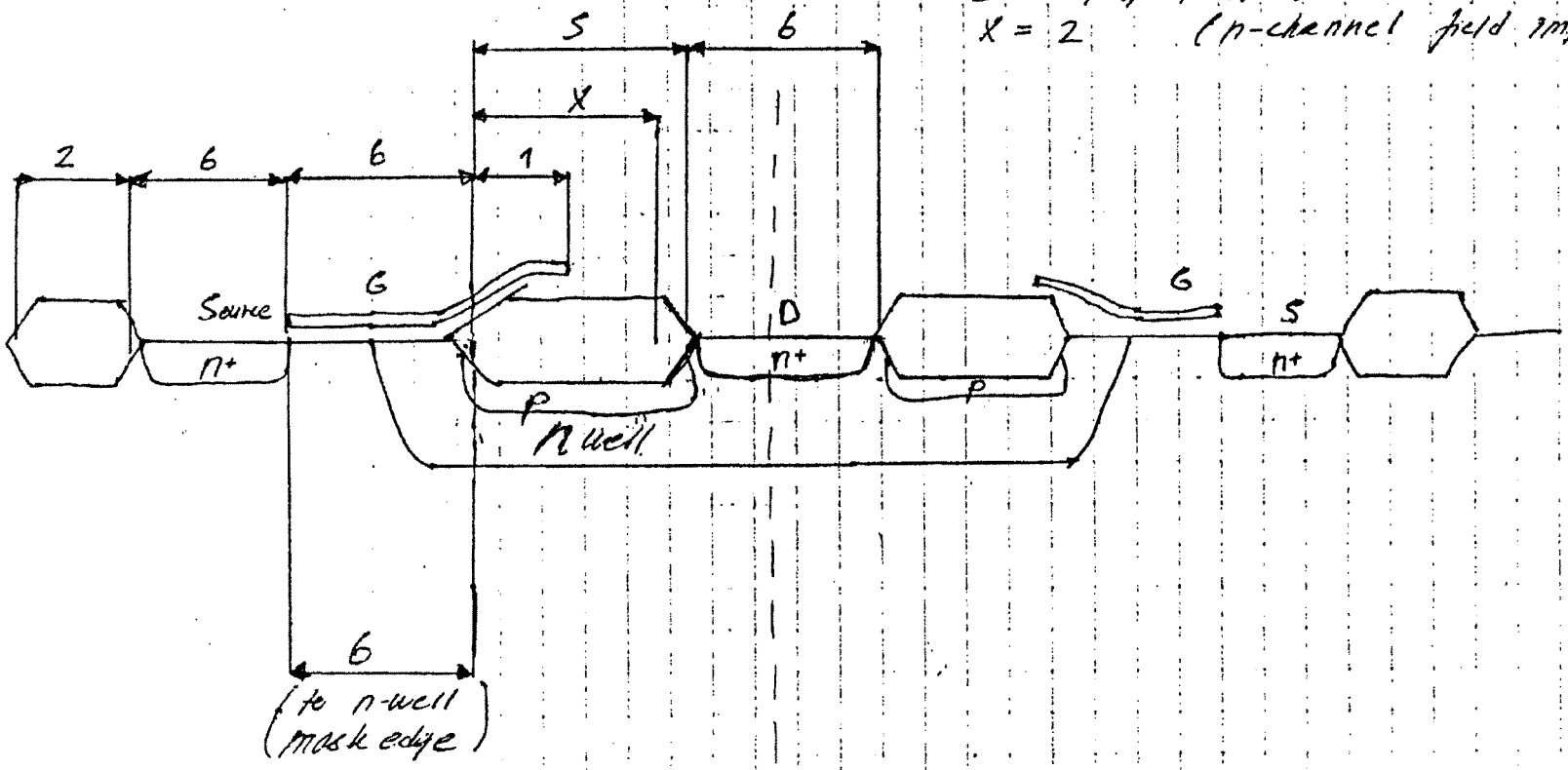


Exhibit B

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HARRIS SEMICONDUCTOR GROUP, BOX 883, MELBOURNE, FLORIDA 32901

This Book is issued by and is returnable to the Library

TECHNICAL RECORD BOOK NO. HS-1298

User's Name JD Beasom

Location

Used from Aug 8 1972 To 19

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LABORATORY NOTEBOOK COMPANY

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HOLYOKE, MASS. 01040

When reordering these books ask for form WW-200-100 with special Harris Semiconductor Label.

ANALOG PRODUCTS DIVISION
GOOD NUMBER LIST
(MISC. OTHER)

DESCRIPTION	MKTG. NO. (DEVICE)	CHARGE NO. (FAMILY)	MASK (PART NO.)	PLH	SIA	ACCOUNTING LEVELS
PRODUCTION						
KEYBOARD ENCODER	0165	5258	1601/10881	2250	AJ6B	01,04,06,07,08,09,15,25,35, 37,40,45,55,56,57,60,65,70, 80,91,92 (ALL LEVELS)
PHASED LOCKED LOOP	2820	5390	5941	2250	AJ6B	01,04,06,07,08,09,15,25,35, 37,40,45,55,56,57,60,65,70, 80,91,92 (ALL LEVELS)
CONDUCTIVITY CELL	55001	5394	1961	2250	AJ6B	01,04,06,07,08,09,15,25,35, 37,40,45,55,56,57,60,65,70, 80,91,92 (ALL LEVELS)

JUN 22 1987

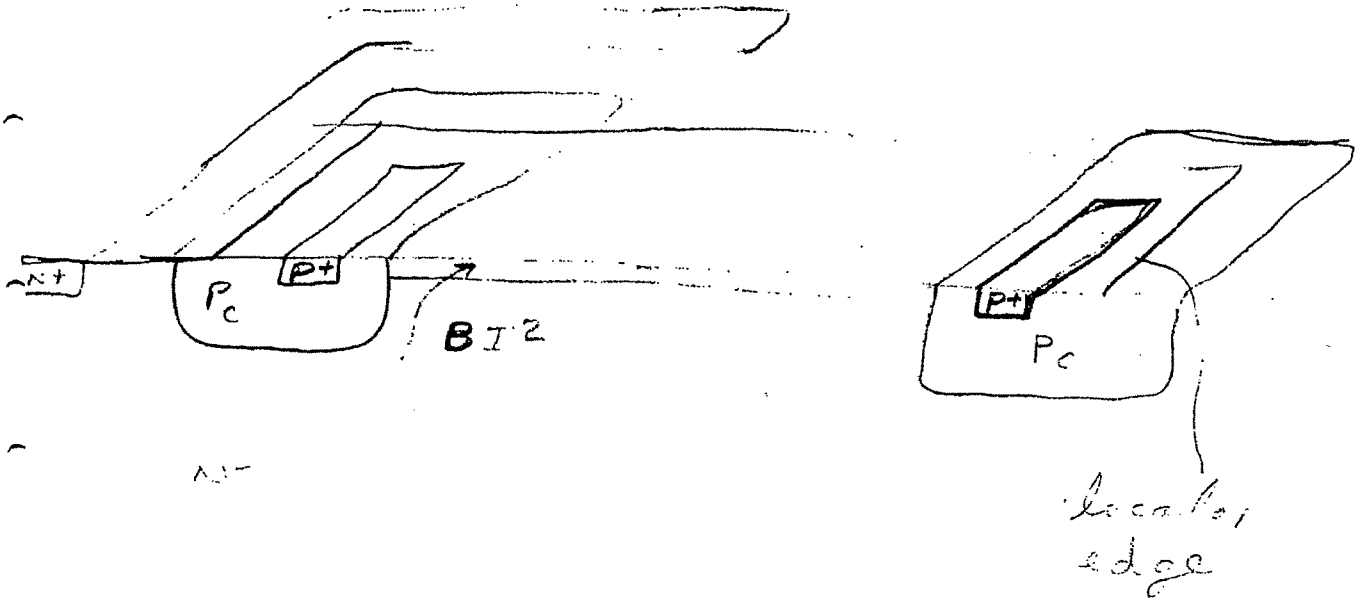
DATE 3/24/82

SIGNED

SIGNED

JO Beason
March 24 1982

High voltage P-n-p transistor only PJFET:



design [illegible] to fully deplete at minimum rather than to breakdown voltage

DATE 3/24/82 SUB-

PROJECT NO.

SIGNED JO Beason

DATE 3/24/82

PROJECT NO.

WITNESSED AND UNDERSTOOD

SIGNED

SIGNED

DATE

DATE

DATE 3/24/82

JO Beeson
Mar 24, 1982

Exhibit C

HARRIS SEMICONDUCTOR SECTOR

	FROM:	DATE:
T. N. Twomey	J. D. Beasom	12/3/84

SUBJECT: Patent Disclosure SE-375

Please find attached a disclosure "A High Voltage Lateral MOS Structure with Reduced On Resistance". Devices of the disclosed type have been designed and included in a test mask set. They may be used in future high voltage analog switch and multiplexer products.

J. D. Beasom

J. D. Beasom

JDB:dg

M124

HIGHLY CONFIDENTIAL

Case No. 04-1371-JJF
DEFT Exhibit No. DX 558
Date Entered _____
Signature _____

FCS1691462

INVENTION CHECKLIST

Instructions: This form is to be used for initial reporting of invention to Division Counsel. Items 1-9 should be completed. Check applicable block(s) in items 3-7. Item 10 will be completed by Counsel and copy returned to Preparer.

1. Date of first written description of the invention: 4/10/84

2. Subject of invention: A high voltage lateral MOS structure with reduced on resistance.

3. Principal category:

[ ] Process
[x] Device
[ ] Circuit
[ ] Other

4. Current status:

[ ] Concept only
[x] Experimental work begun
[ ] Reduced to a practical embodiment

5. Priority:

[ ] High
[x] Moderate
[ ] Low

6. Usage:

[ ] Proposed for use in HSD product
[ ] Currently used in HSD product
[X] Other

7. Date of first publication, offer of sale, or commercial use:

None.

8. Person(s) to contact for additional information:

J. D. Beasom 7567
Telephone Ext.

Telephone Ext.

9. Person who prepared this report:

J. D. Beasom

10. Receipt acknowledged by Counsel:

Date:

A High Voltage Lateral MOS Structure

With Reduced On Resistance

The lateral drift region MOS structure illustrated in Fig. 1 is a known structure which can be used to build high voltage MOS devices. The basic high voltage junction of the structure is the drain body junction.

The drift region is used to connect the high voltage part of the structure to the gate and source which never assume large voltages with respect to the body. The drift region acts as a JFET channel with the underlying MOS body acting as JFET gate. It is designed to totally deplete as the drain body is reverse biased before critical field is reached in the channel to body depletion layer. In this way the drain body breakdown voltage is preserved and the source and gate over gate oxide are shielded from high drain body voltage by the pinched off JFET channel.

The resistance of the lateral drift region JFET channel is in series with the MOS channel resistance, consequently the channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltage, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

The structure described in this disclosure provides the desired reduced channel resistance. The reduction in channel resistance is accomplished by addition of a top gate which lies over the channel to the prior art structure and is illustrated in Fig. 2. The top gate allows total channel doping to be increased because the top gate to channel depletion layer holds some channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. This additional channel charge (ionized channel impurity atoms) causes the reduction in channel resistance.

The top gate must be designed differently than a normal JFET gate. It must be totally depleted at a body (to which it is connected) drain voltage below the breakdown voltage of the junction it forms with the drain which it abuts. It must also totally deplete before the body to channel depletion layer reaches the top gate to channel depletion layer, thus insuring that a large top gate to drain voltage is not developed by punch through action from the body. A normal JFET gate never totally depletes under any operating conditions.

The channel of the JFET drift region must contact the inversion layer MOS surface channel where they meet. One way to achieve this is illustrated in Fig. 3. The top gate and channel are formed by ion implant using an angled implant mask at the channel edge. The angled mask edge causes the channel and top gate implants to curve to the surface as they are progressively retarded by the increasing thickness of the implant mask. Thus the channel comes to the surface beyond the end of the top gate.

Another method to bring the channel into contact with the surface uses diffusion. The channel and top gate are diffused (possibly after deposition by ion implant). The doping levels and diffusion times are chosen such that the channel diffuses beyond the end of the top gate and reaches the surface. This approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the channel.

The top gate should be tied to the body which is the bottom gate of the drift region JFET. A particularly effective way to accomplish this is to overlap the end of the drift region near the MOS channel with the body contact region. To be effective the body contact must be higher in concentration than the channel so that it forms a continuous region horizontally and/or vertically to the body region.

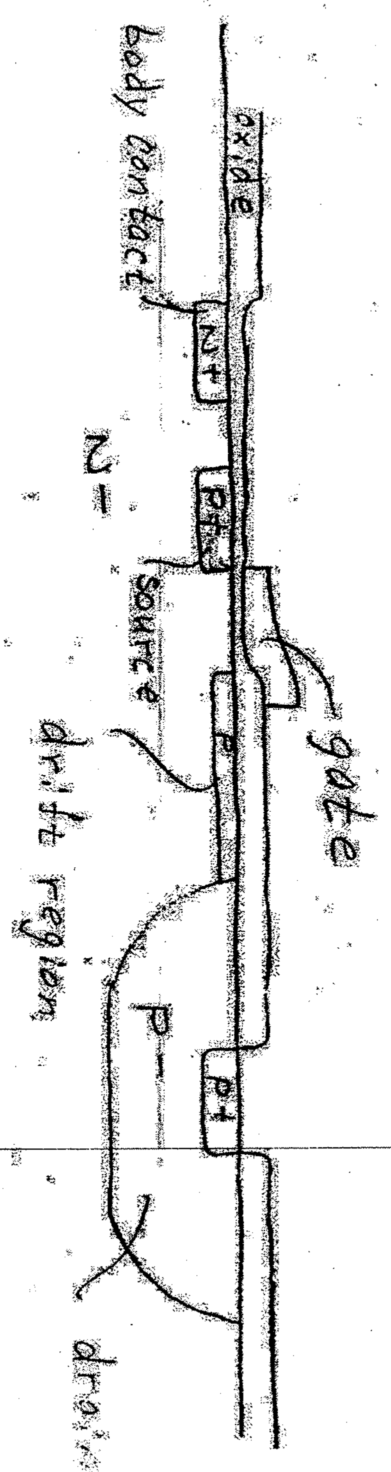


fig 1

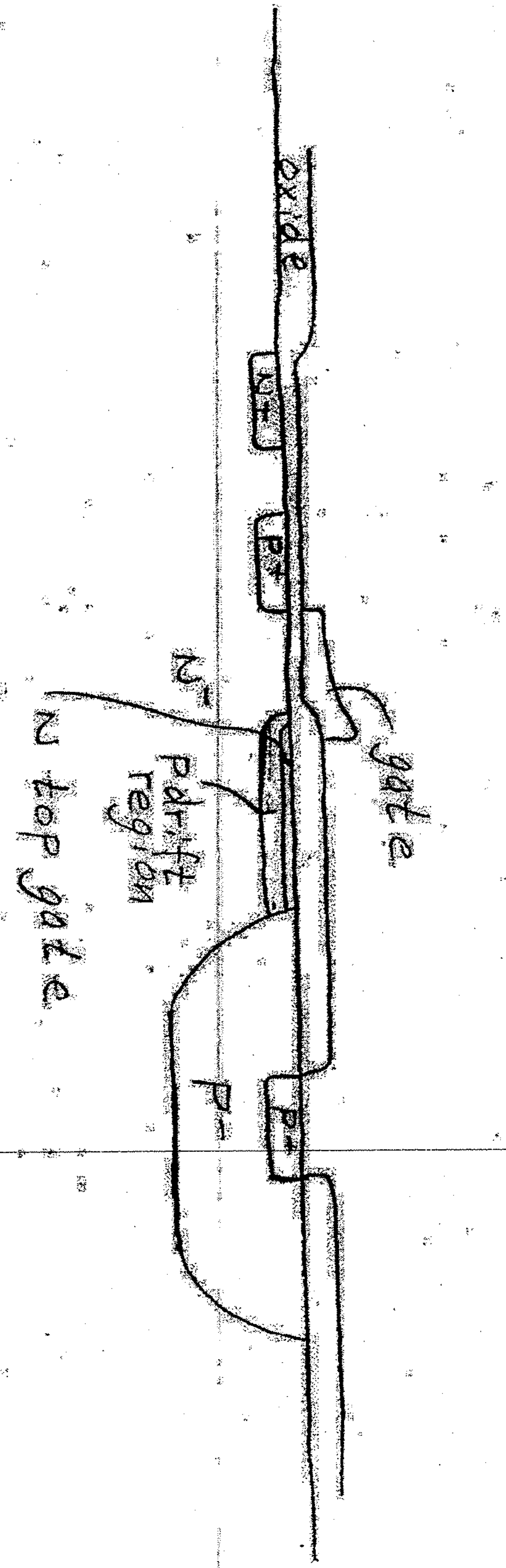
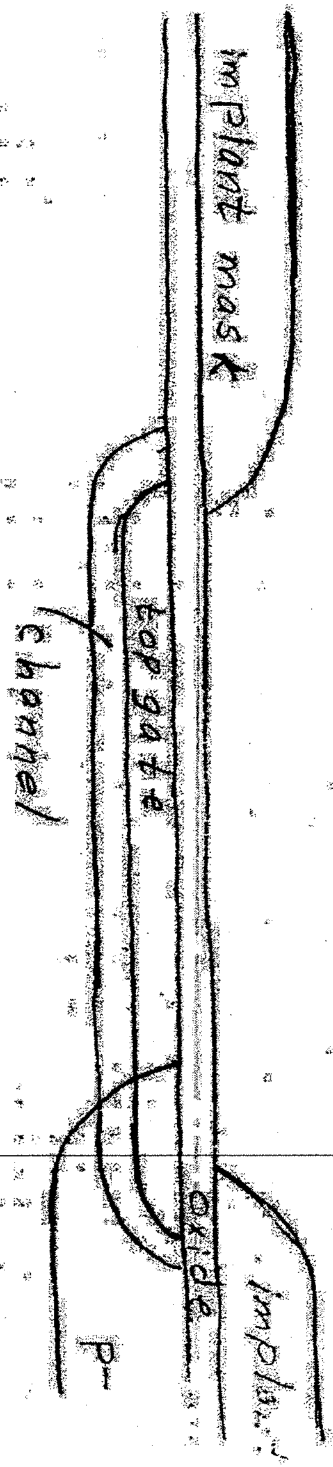


Fig 12



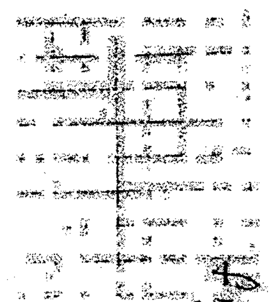


Fig 3

Exhibit D

HARRIS

SEMICONDUCTOR SECTOR

068IV-JDB-28030

TO:	FROM:	DATE
T. N. Twomey	J. D. Beasom	4/24/85

SUBJECT: Broadening of Patent Disclosure SE-395 "A High Voltage Lateral MOS Structure"

The disclosure describes an improvement to lateral drift region type MOS devices. Lateral transistors can also be made using a similar lateral drift region. Such devices are described in the U.S. patents of Sirai (4,288,236) and Sugawara et al (4,419,685).

The same modification which I have disclosed to improve the MOS device can be used to improve the lateral bipolar device. All the same design and structure considerations apply. Fig. 1 illustrates a prior art device and one with the improvement of my disclosure. Fig. 2 illustrates an improved device in which the drift region does not extend all the way to the N emitter shield. The device can also be made as shown in Fig. 2 but with the emitter shield deleted.

Also illustrated in Fig. 2 is use of a deep diffusion to form the collector. This leads to higher breakdown voltage. Either the emitter step (as shown in Fig. 1) or a special step (as shown in Fig. 2) may be used to form the collector. The same is true for source and drain for the MOS device described in the original disclosure. The choice made will depend upon the desired device performance and does not affect the concept of the disclosure.

An extension of the concept which may be used to increase drain-body breakdown for the MOS and collector-base breakdown for the bipolar device is shown in Fig. 3. The drift region extends outward from the entire perimeter of the drain or collector. In this case, it acts to mitigate the breakdown reduction due to junction curvature.

Planar diode breakdown improvement by use of a surface layer of the conductivity type of the surface region (drain or collector in these examples) which extends out from the perimeter of that layer is known prior art. The improvement here is that a common set of process steps produces both a suitable breakdown improvement layer (here N over P or P over N rather than prior art single conductivity type) and an improved drift region.

J. D. Beasom

J. D. Beasom

JDB:dg

M124

HIGHLY CONFIDENTIAL

FCS1691469

Case No. 04-1371-JJF
DEFT Exhibit No. DX 632
Date Entered _____
Signature _____

fig 1

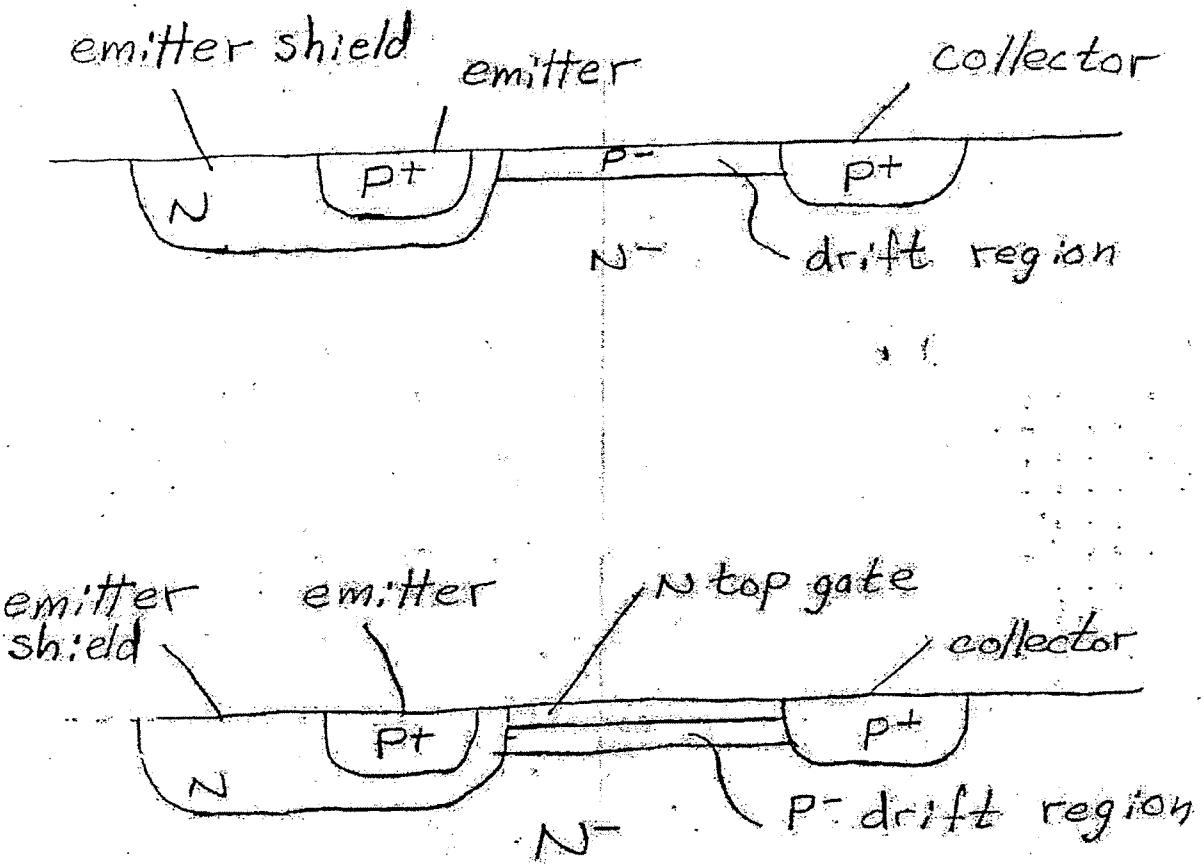

emitter shield
emitter
collector
P+
P-
P+
N
N-
drift region
emitter shield
emitter
N top gate
collector
P+
P+
N
N-
P- drift region

fig 2

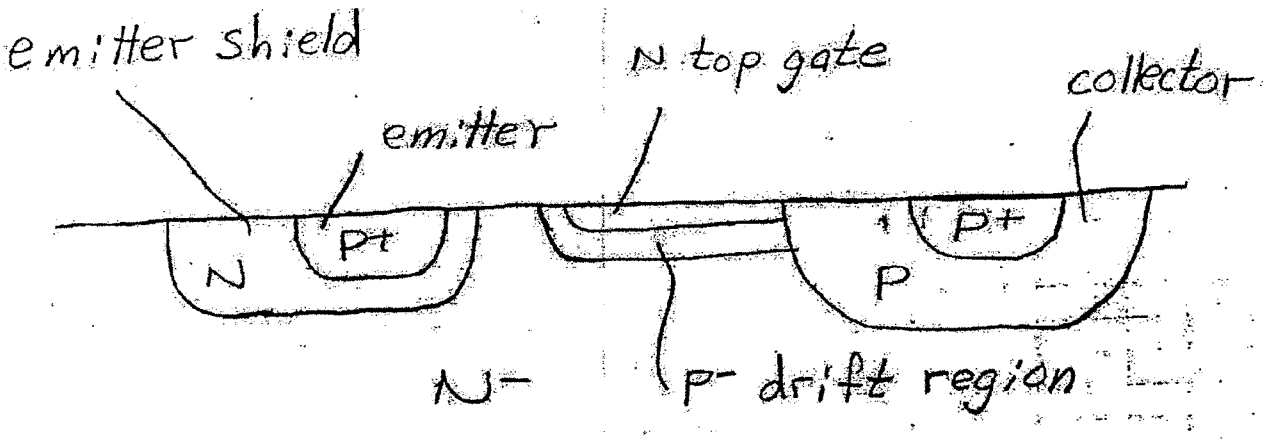
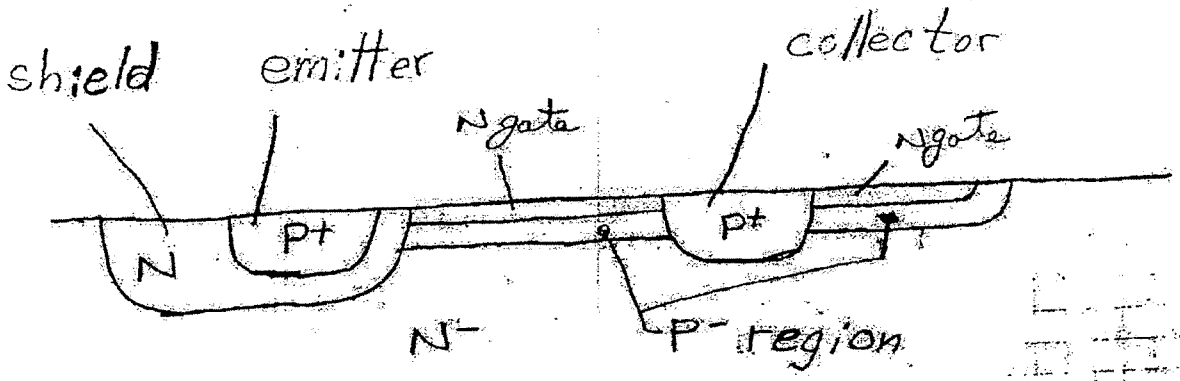
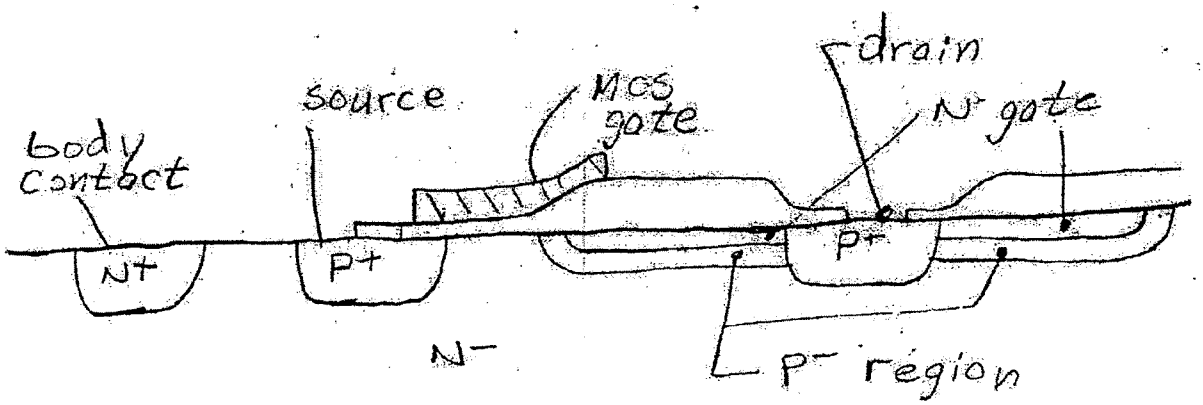

emitter shield
N top gate
collector
emitter
P+
N
P+
P
N-
P- drift region

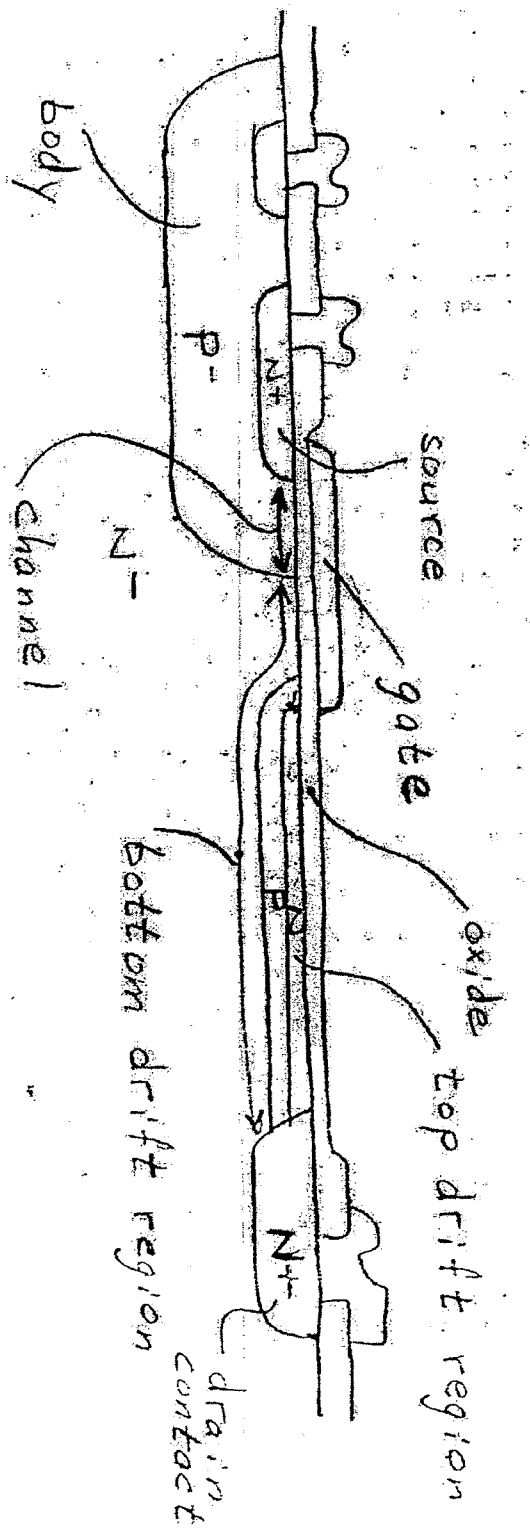
fig 3

Lateral PNP



P channel MOS





Improved lateral Nch DMOS

Exhibit E

From: Jeff Bragalone [jbragalone@ShoreChan.com]
Sent: Monday, January 23, 2006 4:51 PM
To: Michael Headley
Cc: Joseph Depumpo
Subject: RE: PI-Fairchild: Beasom subpoena & production

Michael –

As I mentioned in our phone conference this afternoon, your letter from last Friday is incorrect with respect to Mr. Beasom's compliance with the prior subpoena. The documents that I was referring to in our brief call last week are Intersil documents, for which you issued no subpoena. Accordingly, Mr. Beasom complied fully with the subpoena.

Nevertheless, as a courtesy, I will be sending you via email shortly a copy of one document that we intend to disclose to Mr. Beasom to refresh his recollection in preparation for his deposition. If we ultimately encounter any other documents that we believe should be produced, we will do so either at the deposition or, if practical, in advance.

Under the circumstances, I am unable to see how your client has suffered any prejudice, much less such significant prejudice that would warrant a postponement of the depositions. But, if you still believe that we have somehow prejudiced your client such that the deposition of Mr. Beasom should not go forward, please file a motion to that effect and set an immediate hearing with notice to this firm. Otherwise, we expect the depositions to go forward as noticed and subpoenaed, and we will not be amenable to re-producing any of the subpoenaed witnesses absent a Court order.

I trust this clarifies our position. If you have any questions, or would like to speak further, please feel free to give me a call.

-- Jeff

SHORE CHAN
BRAGALONE LLP
Attorneys & Counselors at Law

Jeffrey R. Bragalone
325 North Saint Paul St.
Suite 4450
Dallas, Texas 75201
214-593-9125 (Direct)
214-593-9110 (Firm)
214-593-9111 (Fax)

From: Michael Headley [mailto:Headley@fr.com]
Sent: Friday, January 20, 2006 9:05 PM
To: Joseph Depumpo; Jeff Bragalone

Subject: Re: PI-Fairchild: Beasom subpoena & production

Joe & Jeff,

Please see attached.
Michael R. Headley
Fish & Richardson P.C.
500 Arguello St., Suite 500
Redwood City, CA 94063-1526
(650) 839-5139 (direct)
(650) 839-5071 (fax)

<<2006 Headley ltr to Bragalone and DePumpo re Beasom subpoena.pdf>>

Exhibit F

ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 MARSH ROAD
MENLO PARK, CA 94025
tel 650-614-7400
fax 650-614-7401
WWW.ORRICK.COM

Brian H. VanderZanden
(650) 614-7629
bvanderzanden@orrick.com

April 24, 2006

VIA FACSIMILE

Michael R. Headley
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Michael:

As I mentioned in my previous letter, Fairchild is working with Intersil to collect any non-privileged documents Intersil may have that are relevant to Power Integrations' discovery requests. Please find the attached documents bearing Bates range FCS1691462 - FCS1691473, all marked Highly Confidential. We received a poor quality copy of these documents Friday, and did not receive a higher quality copy until today. They were not previously in our possession, custody, or control.

Please feel free to contact me with any issues concerning these documents, or any other Intersil documents.

Sincerely,

B. VanderZanden

Brian H. VanderZanden

BHV:ma5

cc: William J. Marsden, Jr.
Howard G. Pollack

HARRIS SEMICONDUCTOR SECTOR

TO:	FROM:	DATE:
T. N. Twomey	J. D. Beasom	12/3/84

SUBJECT: Patent Disclosure SE-375

Please find attached a disclosure "A High Voltage Lateral MOS Structure with Reduced On Resistance". Devices of the disclosed type have been designed and included in a test mask set. They may be used in future high voltage analog switch and multiplexer products.

J. D. Beasom

JDB:dg

M124

INVENTION CHECKLIST

Instructions: This form is to be used for initial reporting of invention to Division Counsel. Items 1-9 should be completed. Check applicable block(s) in items 3-7. Item 10 will be completed by Counsel and copy returned to Preparer.

1. Date of first written description of the invention: 4/10/84

2. Subject of invention: A high voltage lateral MOS structure with reduced on resistance.

3. Principal category:

[ ] Process
[x] Device
[ ] Circuit
[ ] Other

4. Current status:

[ ] Concept only
[x] Experimental work begun
[ ] Reduced to a practical embodiment

5. Priority:

[ ] High
[x] Moderate
[ ] Low

6. Usage:

[ ] Proposed for use in HSD product
[ ] Currently used in HSD product
[x] Other

7. Date of first publication, offer of sale, or commercial use:

None.

8. Person(s) to contact for additional information:

J. D. Beason — 7567 Telephone Ext.

Telephone Ext.

9. Person who prepared this report:

J. D. Beason

10. Receipt acknowledged by Counsel:

Date:

A High Voltage Lateral MOS Structure

With Reduced On Resistance

The lateral drift region MOS structure illustrated in Fig. 1 is a known structure which can be used to build high voltage MOS devices. The basic high voltage junction of the structure is the drain body junction.

The drift region is used to connect the high voltage part of the structure to the gate and source which never assume large voltages with respect to the body. The drift region acts as a JFET channel with the underlying MOS body acting as JFET gate. It is designed to totally deplete as the drain body is reverse biased before critical field is reached in the channel to body depletion layer. In this way the drain body breakdown voltage is preserved and the source and gate over gate oxide are shielded from high drain body voltage by the pinched off JFET channel.

The resistance of the lateral drift region JFET channel is in series with the MOS channel resistance, consequently the channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltage, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

The structure described in this disclosure provides the desired reduced channel resistance. The reduction in channel resistance is accomplished by addition of a top gate which lies over the channel to the prior art structure and is illustrated in Fig. 2. The top gate allows total channel doping to be increased because the top gate to channel depletion layer holds some channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. This additional channel charge (ionized channel impurity atoms) causes the reduction in channel resistance.

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A High Voltage Lateral MOS Structure with Reduced On-Resistance

Another method to bring the channel into contact with the surface uses diffusion. The channel and top gate are diffused (possibly after deposition by ion implant). The doping levels and diffusion times are chosen such that the channel diffuses beyond the end of the top gate and reaches the surface. This approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the channel.

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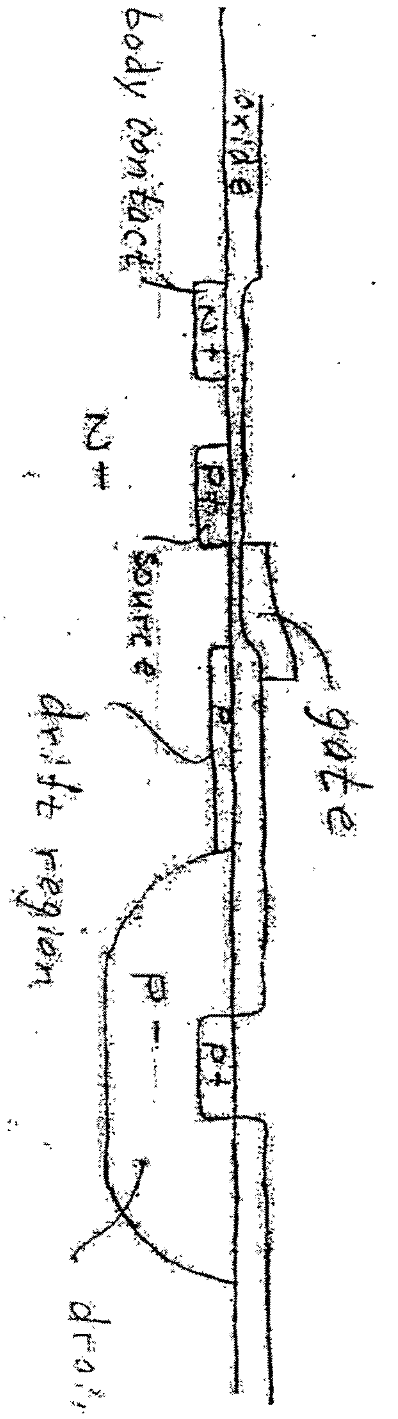
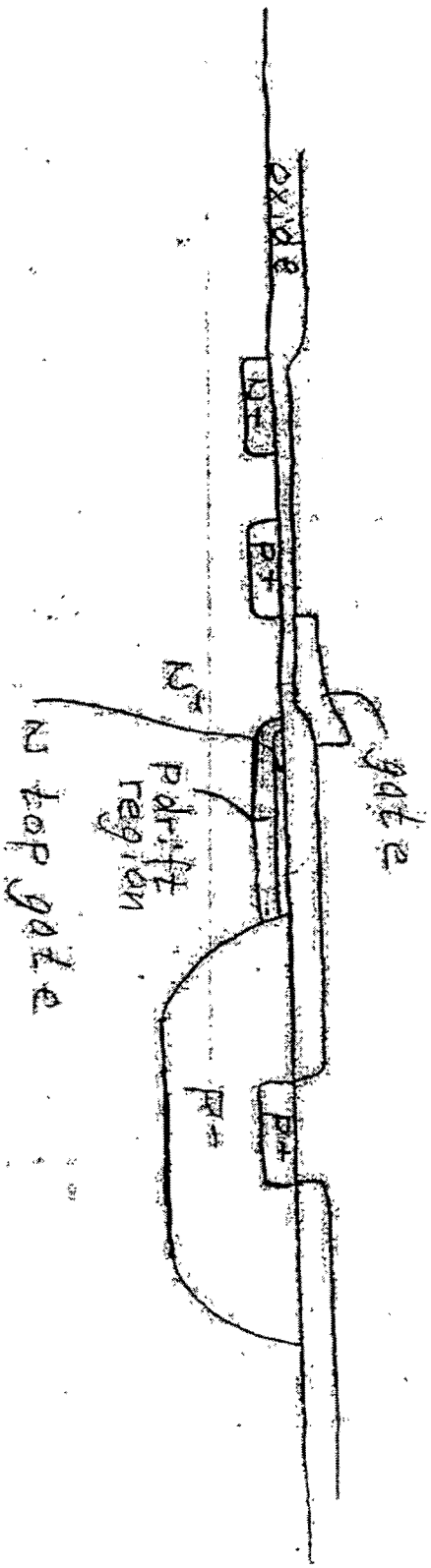
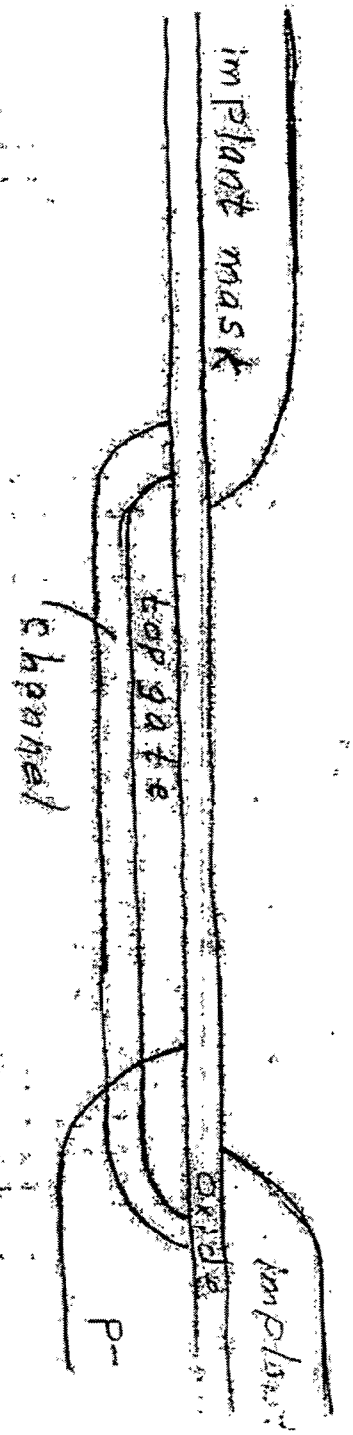


Fig. 1


extra
P+
P+
P+
N top gate
N drift region
gate



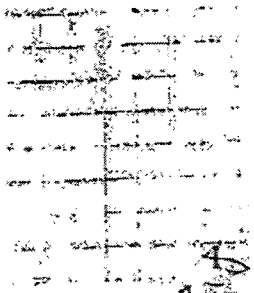


Fig 3

HARRIS SEMICONDUCTOR SECTOR

0681V-JDB-28030

TO:	FROM:	DATE:
T. N. Twomey	J. D. Beason	4/24/85

SUBJECT: Broadening of Parent Disclosure SK-395 "A High Voltage Lateral MOS Structure"

The disclosure describes an improvement to lateral drift region type MOS devices. Lateral transistors can also be made using a similar lateral drift region. Such devices are described in the U.S. patents of Sirvi (4,281,236) and Sugawara et al (4,419,685).

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J. D. Beason

JDB:dg

M124

fig 1

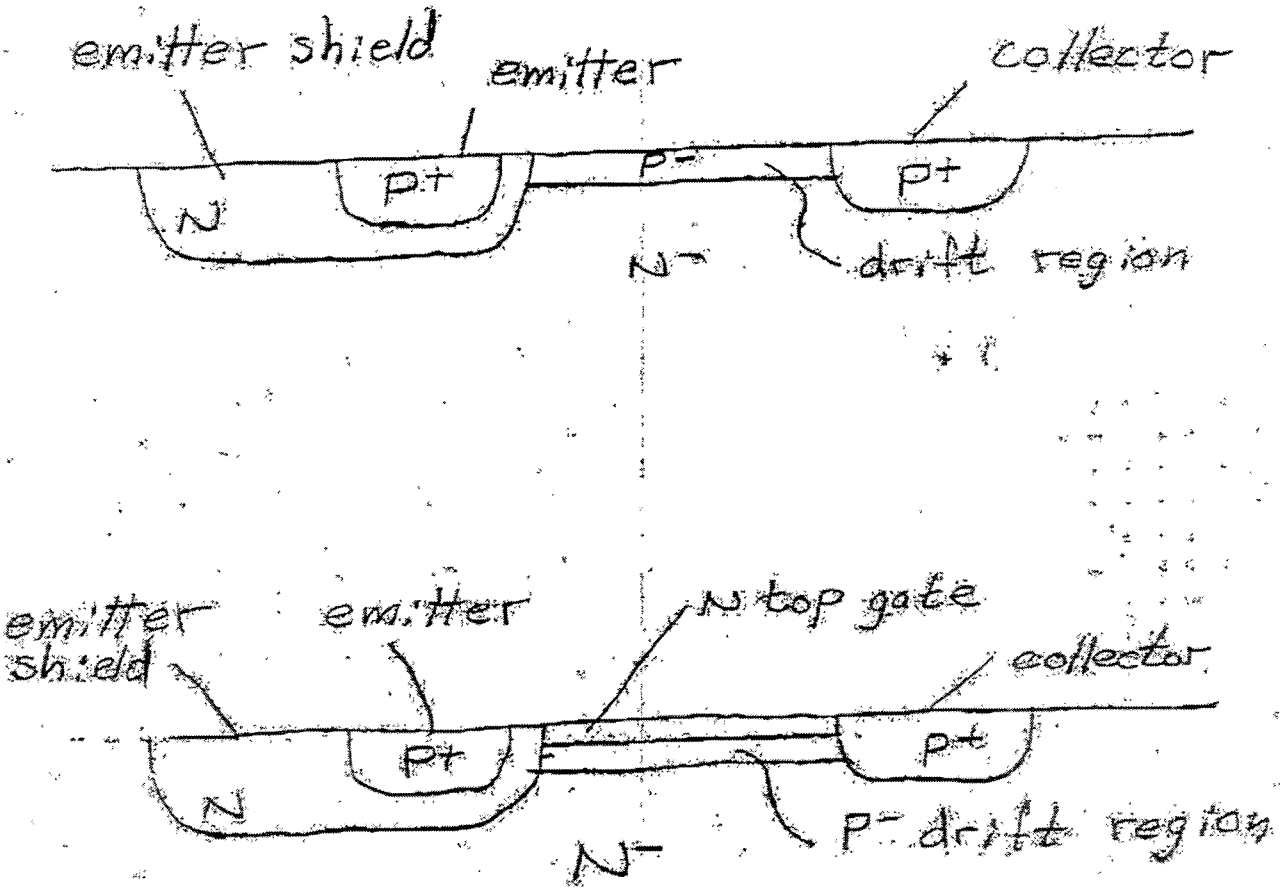

emitter shield
emitter
collector
P+
P-
P+
N
N-
drift region
emitter shield
emitter
N top gate
collector
P+
P+
N
N-
P- drift region

Fig 2

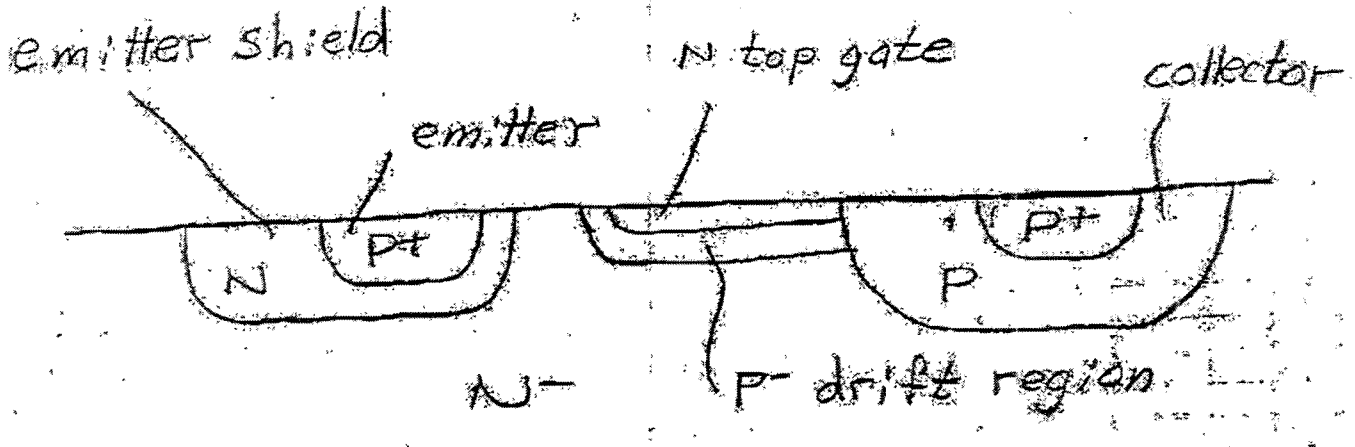
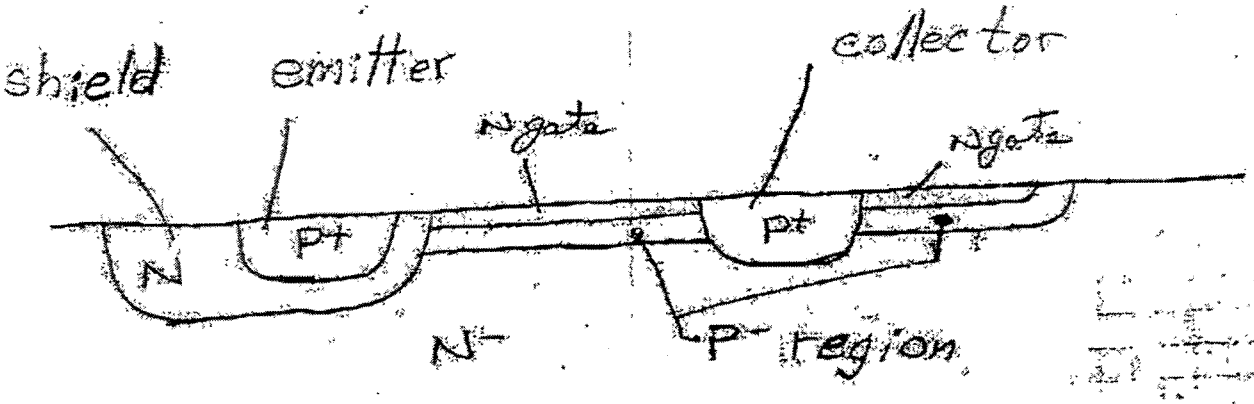
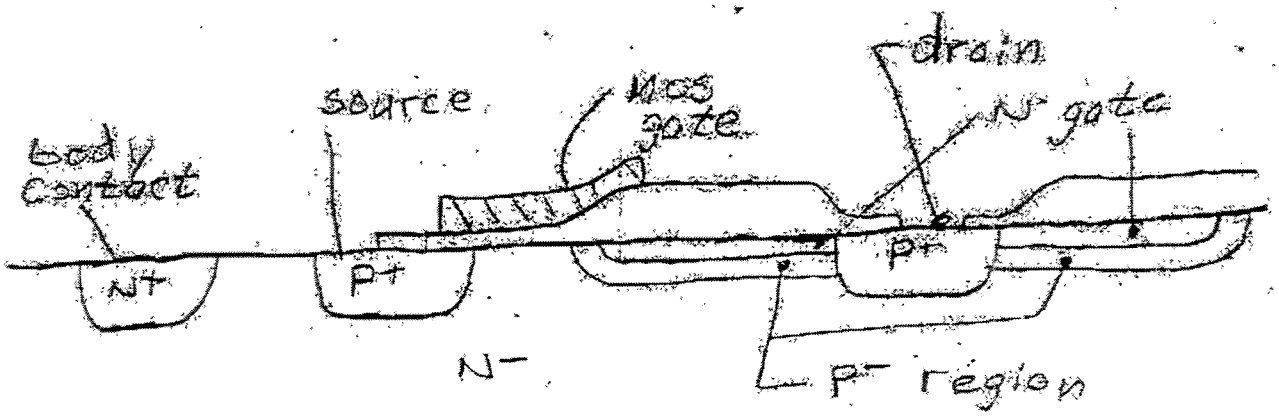

emitter shield
emitter
N top gate
collector
P+
P+
N
P
NJ-
P- drift region

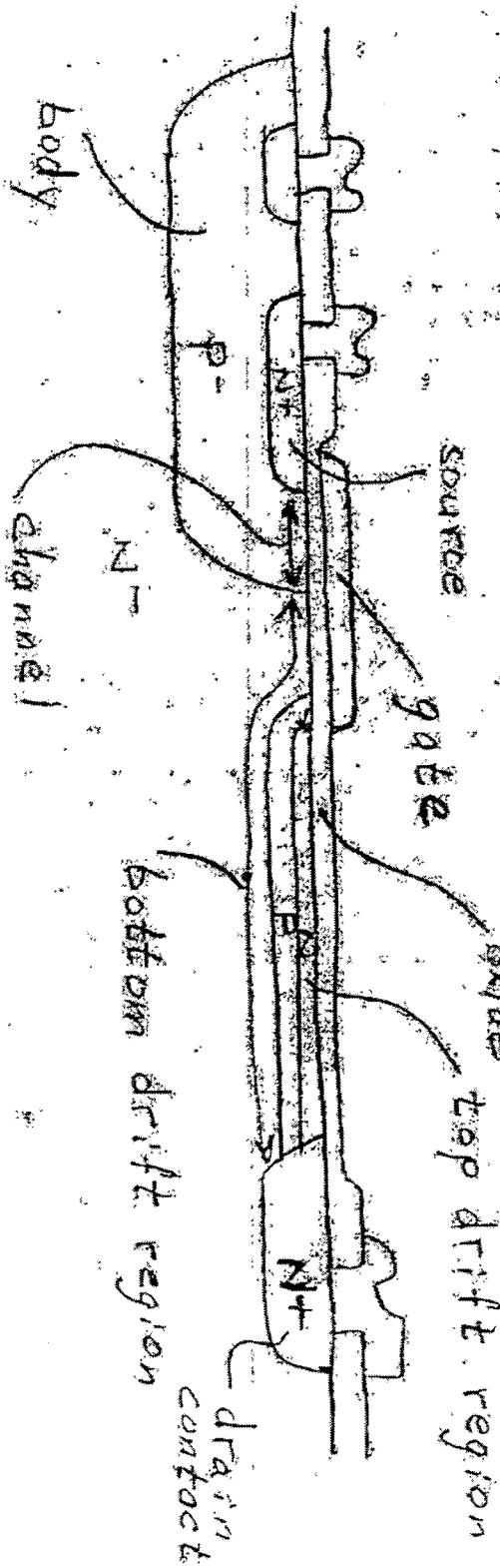
fig 3

Lateral PNP



P channel MOS





Improved lateral N-ch DMOS

ORRICK

ORRICK, HERRINGTON & SUTCLIFFE LLP
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RE *Power Integrations v. Fairchild Semiconductor, et al.*

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